California University of Pennsylvania
University Course Syllabus
Approved: Spring 2006

Department of Mathematics, Computer Science and Information Systems

A. Protocol

Course Name:	Logic and Switching Theory of the Computer
Course Number:	CSC 216
Credits:	3
Prerequisites:	MAT 195 Discrete Mathematical Structures with C- or better

Maximum Class Size (face-to-face): 35
Maximum Class Size (online): N.A.

B. Objectives of the Course:
Upon completion of this course the student will be able to:

1) Perform numerical conversions of any base.
2) Identify and convert various non-weighted codes.
3) Identify and convert various weighted codes.
4) Perform binary arithmetic operations.
5) Identify functional components.
6) Form combinational networks and expressions.
7) Construct network diagrams.
8) Convert between normal and standard Boolean forms.
9) Identify and apply Boolean connectives.
10) Apply combinational network analysis and synthesis.
11) Apply the Karnaugh Map minimization technique.
12) Apply the Quine-McCluskey minimization technique.
13) Minimize switching functions with don't care states.
14) Translate networks into all NAND or all NOR logic.
15) Create timing diagrams for sequential networks.
16) Form state transition tables and diagrams.
17) Perform analysis and synthesis of latches and flip-flops.
18) Perform analysis and synthesis of sequential networks.
19) Perform analysis and synthesis of asynchronous networks.
20) Identify encoders, decoders, transcoders, multiplexers, demultiplexers, ROMs and PLAs.

C. Catalog Description:
This course provides the student with an in-depth study of the basis of digital computers. Number systems, arithmetic operations, codes, boolean algebra, boolean minimization techniques, state transition tables, and state transition graphs are discussed. Extensive emphasis is placed on the analysis and synthesis of synchronous and asynchronous combinational networks which form digital computers. Pre requisite: MAT 195 Discrete Mathematical Structures with C- or better. Three credits.

D. Outline of the Course:
1) Numbers
    a. Introduction and Representation of Information
        i. Representation based on distinguish ability
        ii. Representation based on application
        iii. Representation based on arithmetic
        iv. Representation based on error control
    b. Integer Base Conversion
        i. Binary to decimal

ii. Base x to decimal
iii. Decimal to binary
iv. Decimal to base x

c. Fraction Base Conversion
i. Binary to decimal
ii. Base x to decimal
iii. Decimal to binary
iv. Decimal to base x

d. Notations and Conversions
i. Hexadecimal and binary
ii. Octal and binary
iii. Base y and base x

e. Codes and Conversions
i. Non-weighted codes
(1) ASCII
(2) EBCDIC
(3) Gray
(4) Parity
ii. Weighted codes
(1) BCD
(2) 2421
(3) 642-3
(4) 2-out-of-5

f. Binary Arithmetic operations
i. Addition
ii. Subtraction
iii. Sign magnitude
iv. 1's complement notation
v. 2's complement notation

2) Binary Functions

a. Functional components
i. Combinational
ii. Storage

b. Switching functions
i. AND
ii. OR
iii. INVERTER
iv. NAND
v. NOR
vi. XOR
vii. XNOR

c. Combinational networks and expressions
i. Network diagrams
ii. Expressions

d. Switching Algebra
i. Boolean connectives
ii. DeMorgan
iii. Normal form
iv. Standard form

3) Combinational Networks

a. Analysis
b. Synthesis
c. Translate Networks to all NANDs or all NORs

4) Minimization Techniques

a. Karnaugh maps
b. Karnaugh maps and don't cares
c. Quine-McCluskey

d. Quine-McCluskey and don't cares

5) Combinational Modules
   a. Encoders
   b. Decoders
   c. Transcoders
   d. Multiplexers
   e. Demultiplexers
   f. ROMs
   g. PLAs

6) Synchronous Sequential Networks
   a. Timing diagrams
   b. Latch (Flip Flops)
      i. RS
      ii. Master Slave
      iii. D
      iv. JK
      v. T
   c. Registers
   d. Analysis of sequential networks
      i. State transition tables
      ii. State transition diagrams
   e. Synthesis of sequential networks
      i. Stuck states
      ii. Two level (AND OR) design
      iii. Design using combinational modules
   f. Asynchronous Sequential Networks
      i. Analysis
      ii. Synthesis

E. Teaching Methodology:

1) Traditional Classroom Methodology:
This course will be taught using the lecture/discussion method and cooperative group method during appropriate sections of the course.

2) Online Methodology:
This course will not be taught online.

F. Text:
Clements Principles of Computer Hardware (4^{th} Edition) ISBN 0199273138

G. Assessment Activities:

1) Traditional Classroom Assessment
The final grade will be determined as a percentage from the following evaluation methods with varying weights at the discretion of the instructor:

   a. Examinations
   b. Quizzes
   c. Assignments
   d. Programs
   e. Attendance
   f. Performance

2) Online Assessment
No online assessments will be given.

H. Accommodations for Students with Disabilities:

Accommodations for Students with Disabilities

Students reserve the right to decide when to self-identify and when to request accommodations. Students requesting approval for reasonable accommodations should contact the Office for Students with Disabilities (OSD). Students are expected to adhere to OSD procedures for self-identifying, providing documentation and requesting accommodations in a timely manner.
Students will present the OSD Accommodation Approval Notice to faculty when requesting accommodations that involve the faculty.

Contact Information:

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